We claim:

1. An integrated circuit for use in a transceiver module, the integrated circuit comprising:

a first electrical input port for receiving a first serial electrical data stream;

receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream;

a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;

receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream;

a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;

transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and

a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.

2. The integrated circuit of claim 1 wherein the bypass data path is selected when the first serial electrical data stream has a data rate below a predetermined threshold.

3. The integrated circuit of claim 2 wherein:

the receiver eye opener circuitry has a data rata range including 10 Gb/s; and

the bypass data path is selected when the first serial electrical data stream has a data rate below approximately 3 Gb/s.

4. The integrated circuit of claim 1 wherein the bypass data path is selected when the first serial electrical data stream has a data rate that is not within a data rate range of the receiver eye opener circuitry.

5. The integrated circuit of claim 1 wherein the bypass data path is selected in response to a loss of lock (LOL) signal.

6. The integrated circuit of claim 1 wherein the bypass data path is selected in response to a loss of signal (LOS) signal.

7. The integrated circuit of claim 1 wherein the bypass data path is selected in response to a command received from external to the integrated circuit.

8. The integrated circuit of claim 1 further comprising:

bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path.

9. The integrated circuit of claim 1 wherein the receiver bypass circuitry comprises an adaptive equalizer.

10. The integrated circuit of claim 1 further comprising:

power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected.

11. In an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a first serial electrical data stream;

switchably selecting or not selecting a bypass data path;

retiming and reshaping the first serial electrical data stream when the bypass data path is not selected;

passing through the first serial electrical data stream when the bypass data path is selected;

transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit when the bypass data path is not selected, or transmitting the passed-through first serial electrical data stream to external to the integrated circuit when the bypass data path is selected;

receiving a second serial electrical data stream from external to the integrated circuit;

retiming and reshaping the second serial electrical data stream; and

transmitting the retimed and reshaped second serial electrical data stream.

12. The method of claim 11 wherein the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate below a predetermined threshold.

13. The method of claim 11 wherein the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate that is not within a data rate range of the step of retiming and reshaping.

14. The method of claim 11 wherein the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path in response to a loss of lock (LOL) signal.

15. The method of claim 11 wherein the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path in response to a loss of signal (LOS) signal.

16. An integrated circuit for use in a transceiver module, the integrated circuit comprising:

first eye opener means for retiming and reshaping a received first serial electrical data stream;

output means for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;

bypass means for switchably selecting a bypass data path to the output means but bypassing retiming and reshaping of the first serial electrical data stream;

input means for receiving a second serial electrical data stream from external to the integrated circuit;

second eye opener means for retiming and reshaping the second serial electrical data stream.

17. An integrated circuit for use in a transceiver module, the integrated circuit comprising:

an electrical input port for receiving a serial electrical data stream;

an electrical output port for transmitting a retimed and reshaped serial electrical data stream to external to the integrated circuit;

receiver eye opener circuitry for retiming and reshaping the serial electrical data stream, the receiver eye opener circuitry including at least two data paths for the serial electrical data stream, each data path having a different data rate range; and

selection circuitry for switchably selecting the data path that has a data rate range compatible with a data rate of the serial electrical data stream.

18. The integrated circuit of claim 17 wherein each data path comprises:

clock and data recovery (CDR) circuitry, wherein the data rate range of each data path is determined by the data rate range of the CDR circuitry.

19. The integrated circuit of claim 17 further comprising:

rate detection circuitry for determining the data rate of the serial electrical data stream.

20. The integrated circuit of claim 17 further comprising:

receiver bypass circuitry for switchably selecting a bypass data path from the electrical input port to the electrical output port but bypassing retiming and reshaping of the serial electrical data stream.

21. The integrated circuit of claim 17 further comprising:

power management circuitry for powering down the data paths that are not selected.

22. In an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a serial electrical data stream;

switchably selecting a data path that has a data rate range compatible with a data rate of the serial electrical data stream;

retiming and reshaping the serial electrical data stream within the selected data path; and

transmitting the retimed and reshaped serial electrical data stream to external to the integrated circuit.

23. An integrated circuit for use in a transceiver module, the integrated circuit comprising:

input means for receiving a serial electrical data stream;

output means for transmitting a retimed and reshaped serial electrical data stream to external to the integrated circuit;

eye opener means for retiming and reshaping the serial electrical data stream, the eye opener means including at least two data paths for the serial electrical data stream, each data path having a different data rate range; and

selection means for switchably selecting the data path that has a data rate range compatible with a data rate of the serial electrical data stream.